Superimposed voltage tests on DC cables

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ABSTRACT

To generate superimposed/composite test voltages which is a type test requirement, coupling and protection devices have to be integrated into the test circuit with the HVDC cable. Different test circuits are proposed in [1].
The advantages and disadvantages of the spark gap coupling versus the capacitive coupling and the different designs of the protection resistor are discussed. The spark gap coupling results in a cable discharging during the period the impulse voltage is applied, the schematic wave shape representations as per [2] and [3] will only be achieved with the capacitive coupling.
To measure the applied voltage stress on a HVDC cable correctly during the superimposed test the use of a composite measuring system is necessary and now normative. The technical requirements of an appropriate composite measuring system which consists of a RCR divider and a data acquisition system are outlined.
Additional to the HVDC cables application the need to test HVDC gas-insulated test objects (switchgear, instrument transformers) with superimposed (composite) voltages is discussed in the CIGRE JWG D1/B3.57 [4].
At the end, it is the responsibility of the cable/GIS expert community to decide if compromises with respect to the superimposed voltage waveforms can be permitted without questioning the validity of the superimposed voltage test on HVDC cables as per [2], [3] or on GIS.

KEYWORDS

Superimposed voltage test, spark gap coupling, capacitive coupling, protection devices, composite measuring system, data acquisition, bandwidth, analogue bandwidth, rise time, sampling rate, signal resolution, memory depth

INTRODUCTION

After the long duration test of a HVDC cable the integrity of the insulation system is checked by applying a superimposed impulse test. Based on [2] and [3] superimposed voltage tests as type test are requested for HVDC cables. Depending on the cable usage in VSC DC lines (Voltage Source Converter) or in LCC DC lines (Line Commutated Converter) different superimposed impulse test type test procedures are required. Fig. 1, Fig. 2 and Fig. 4 show the different test procedures and the test voltage levels to be applied. Fig. 3 shows the schematic representations of the superimposed voltage test wave shapes to be applied on the HVDC cable.

	SI	RP	SI	RP	LI	RP	LI	SDT
Duration/number	10	24 h Optional, according to 8.8	10	Optional, according to 8.8	10	24 h Optional, according to 8.8	10	2 h
Impulse voltage	–		+		–		+	n.a.
	U_{p2O}		U_{p2O}		U_{p1}		U_{p1}	
DC test voltage	+		–		+		–	–
	U_0		U_0		U_0		U_0	U_T

SI = switching impulse, RP = rest period, LI = lightning impulse, SDT = subsequent DC test

Fig. 1: Superimposed type test procedure for LCC usage according to [2]

	SI	SI	RP	SI	SI	RP	LI	RP	LI	SDT
Duration/number	10	10	24 h Optional, according to 8.8	10	10	24 h Optional, according to 8.8	10	24 h Optional, according to 8.8	10	2 h
Impulse voltage	+	–		–	+		–		+	n.a.
	U_{p2S}	U_{p2O}		U_{p2S}	U_{p2O}		U_{p1}		U_{p1}	
DC test voltage	+	+		–	–		+		–	–
	U_0	U_0		U_0	U_0		U_0		U_0	U_T

SI = switching impulse, RP = rest period, LI = lightning impulse, SDT = subsequent DC test

Fig. 2: Superimposed type test procedure for VSC usage according to [2]

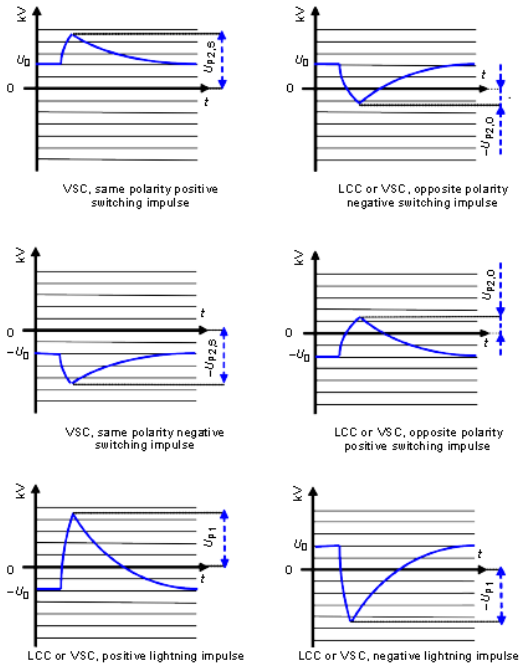

Fig. 3: Schematic representations of the superimposed voltage test wave shapes according to [2], [3]

	same polarity (pos. DC + pos. SI)			opposite polarity (pos. DC + neg. SI)			same polarity (neg. DC + neg. SI)			opposite polarity (pos. DC + neg. SI)			neg. DC + pos. LI			pos. DC + neg. LI		
U_{DC}	$U_{p2,s}$	$U_{p2,s}/U_{DC}$	$+U_{SI}$	$-U_{p2,o}$	$-U_{p2,o}/U_{DC}$	$-U_{SI}$	$-U_{p2,s}$	$-U_{p2,s}/-U_{DC}$	$-U_{SI}$	$U_{p2,o}$	$U_{p2,o}/U_{DC}$	U_{SI}	U_{p1}	U_{p1}/U_{DC}	U_{LI}	$-U_{p1}$	$-U_{p1}/U_{DC}$	U_{LI}
80	168	2.10	88	-96	-1.20	-176	-168	2.10	-88	96	-1.20	176	168	2.10	248	-168	-2.10	-248
150	315	2.10	165	-180	-1.20	-330	-315	2.10	-165	180	-1.20	330	315	2.10	465	-315	-2.10	-465
160	336	2.10	176	-192	-1.20	-352	-336	2.10	-176	192	-1.20	352	336	2.10	496	-336	-2.10	-496
270	567	2.10	297	-324	-1.20	-594	-567	2.10	-297	324	-1.20	594	567	2.10	837	-567	-2.10	-837
320	672	2.10	352	-384	-1.20	-704	-672	2.10	-352	384	-1.20	704	672	2.10	992	-672	-2.10	-992
400	840	2.10	440	-480	-1.20	-880	-840	2.10	-440	480	-1.20	880	840	2.10	1240	-840	-2.10	-1240
525	1103	2.10	577.5	-630	-1.20	-1155	-1103	2.10	-578	630	-1.20	1155	1103	2.10	1628	-1103	-2.10	-1628
600	1260	2.10	660	-720	-1.20	-1320	-1260	2.10	-660	720	-1.20	1320	1260	2.10	1860	-1260	-2.10	-1860
640	1344	2.10	704	-768	-1.20	-1408	-1344	2.10	-704	768	-1.20	1408	1344	2.10	1984	-1344	-2.10	-1984
800	1680	2.10	880	-960	-1.20	-1760	-1680	2.10	-880	960	-1.20	1760	1680	2.10	2480	-1680	-2.10	-2480

Fig. 4: Superimposed test voltage levels as per [2] (yellow area) and as per common practice for HVDC cables up to 800 kV class