SENSITIVITY OF HVDC EXTR CABLE SYSTEM AND IMPLICATIONS ON TESTING

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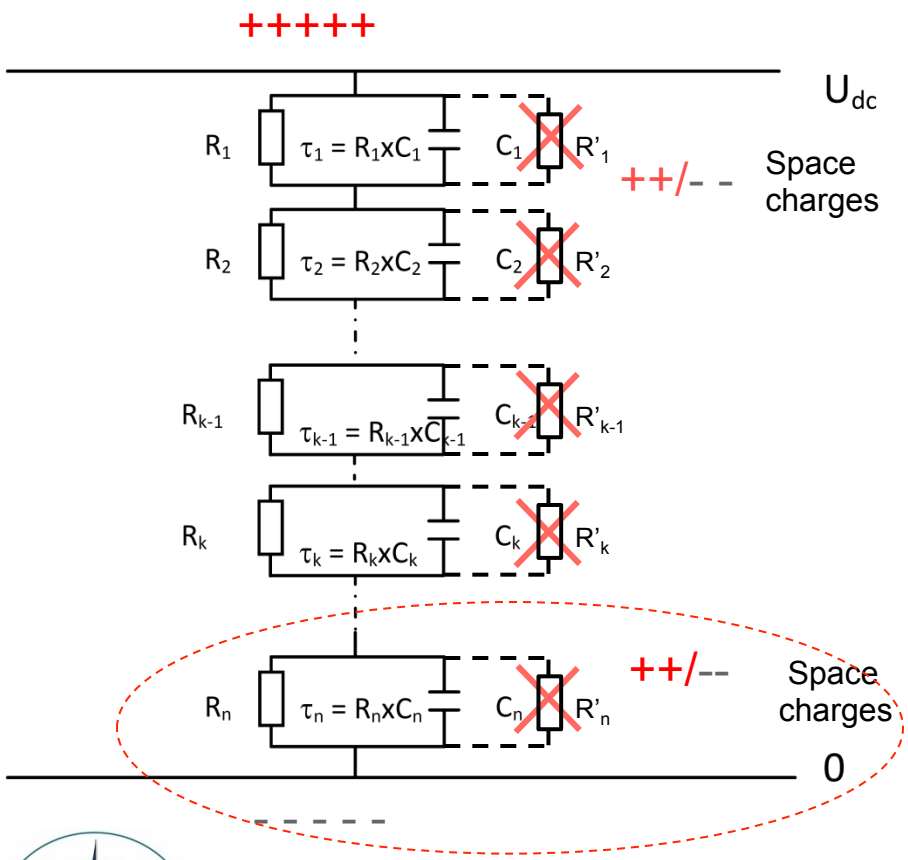
DC Cable Insulation Model



- Under DC, the electrode charges are constant in the stationary case but not constant during transient periods
  - the charges have time enough to move through the very high insulation resistance in sometimes a very complicated manner.
  - Some charges may “remain” in parts of the insulation and create a complicated field distribution due to “space charge build-up”.

Typical BD location in HVDC termination (joint)

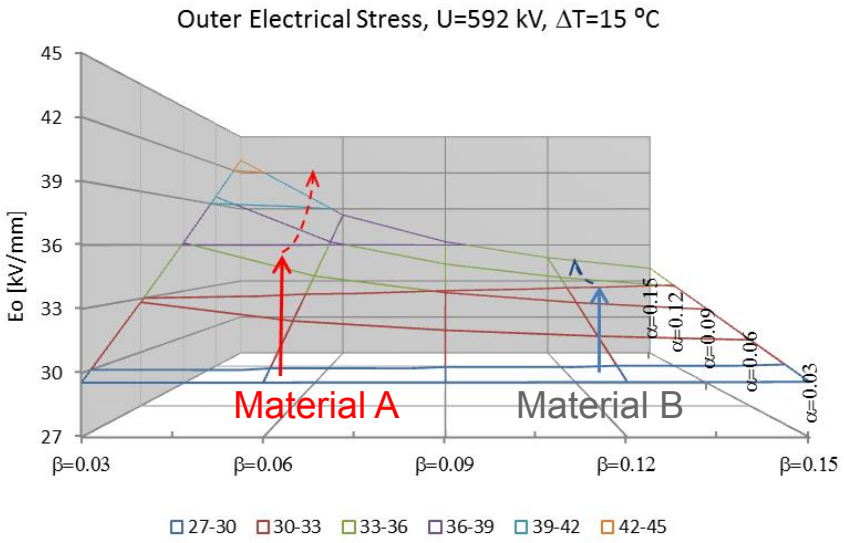
Build-up of charges along interface

Typical DC breakdown some cm's from OSC screen edge

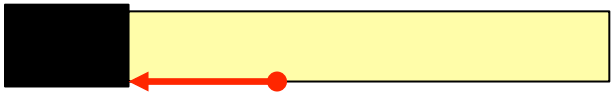
Example - sensitivity of α and β in cable and interfaces

Cable

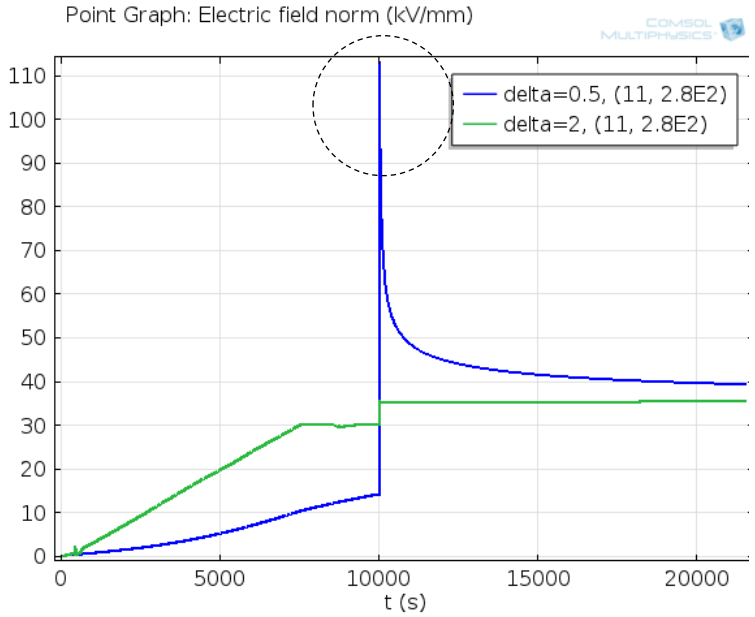
$$\sigma = \sigma_0 e^{\left(\alpha T + \beta |E| + \ldots\right)}$$



Interface



25 mm / 1 s



Background and Questions

- Background:
  A requirement for U > 320 kV, preventing thermal run-away, is a sufficiently low conductance. The interfaces/accessories seem however primarily being dependent on other mechanisms. The cable/interface characteristics is most likely dependent on both cable and interface quality, leaning at higher importance put on the cable characteristics. AC-materials have quite equal material characteristics. DC-materials are numerous now and completely different from each other, especially due to "unknown" time constants etc.
- Questions:

1. Can all HVDC materials be treated under the same system umbrella, i.e. the same TT and PQ requirements for > 320 kV?

2. What are the interface implications on the long term effects at U > 320 kV especially for low conductive DC-materials?

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